CLAIMS

What is claimed is:

1. A method for fabricating a semiconductor die assembly comprising first and second semiconductor dice, the method comprising:

providing a base lead frame having a die attach site with a first side and a second, opposing side and a plurality of primary lead fingers extending away from the die attach site;

attaching a first semiconductor die by a back side thereof to the first side of the die attach site with an active surface of the first semiconductor die facing away from the base lead frame

attaching a second semiconductor die by a back side thereof to the second side of the die attach site with an active surface of the second semiconductor die facing away from the base lead frame;

attaching lead fingers of a first offset lead frame extending over the first semiconductor die to primary lead fingers of the base lead frame;

attaching lead fingers of a second offset lead frame extending over the second semiconductor die to primary lead fingers of the base lead frame; and

electrically connecting lead fingers of the first and second offset lead frames to bond pads of the first and second semiconductor dice.

2. The method of claim 1, further comprising forming the lead fingers of the first and second offset lead frames to respectively extend in a cantilevered manner over the first and second semiconductor dice from locations of attachment of the lead fingers of the first and second offset lead frames to the primary lead fingers.

3. The method of claim 1, further comprising cantilevering the lead fingers of the first and second offset lead frames respectively over the first and second semiconductor dice from location of attachment of the lead fingers of the first and second offset lead frames to the primary lead fingers.

4. The method of claim 1, wherein electrically connecting comprises a technique selected from the group comprising wire bonding, TAB bonding and thermocompression bonding.

5. The method of claim 1, further comprising configuring the first and second semiconductor dice with substantially centrally located bond pads.

6. The method of claim 5, further comprising configuring the first and second semiconductor dice as substantially identical dice.

7. The method of claim 6, further comprising configuring the substantially identical dice as memory dice.

8. The method of claim 1, further comprising:

configuring the base lead frame with first and second groups of primary lead fingers extending away from the die attach site on opposing sides thereof, the primary lead fingers of each group of the base lead frame being laterally spaced and mutually connected by a dam bar extending substantially transversely therebetween;

configuring the first offset lead frame with first and second groups of lead fingers, the lead fingers of each group of the first offset lead frame being laterally spaced and mutually connected by a dam bar extending substantially transversely therebetween, the dam bars of the first offset lead frame being mutually spaced so as to be alignable in superimposition with the dam bars of the base lead frame;

configuring the second offset lead frame with first and second groups of lead fingers, the lead fingers of each group of the second offset lead frame being laterally spaced and mutually connected by a dam bar extending substantially transversely therebetween, the dam bars of the second offset lead frame being mutually spaced so as to be alignable in superimposition with the dam bars of the base lead frame; and

wherein attaching the lead fingers of the first and second offset lead frames to the primary lead fingers of the base lead frame includes aligning the dam bars of the first and second groups of lead fingers of the first and second offset lead frames in superimposition with, and on opposing sides of, the dam bars of the first and second groups of primary lead fingers of the first lead frame.

9. The method of claim 8, further comprising placing cavities of opposing transfer mold dies over opposing sides of the base lead frame with outer borders of the cavities on opposing sides of the die attach site being located immediately adjacent the superimposed dam bars of the first and second offset lead frames and the base lead frame.

10. The method of claim 9, further comprising locating the outer borders of the die cavities on outer surfaces of the dam bars of the first and second offset lead frames.

11. The method of claim 9, further comprising injecting a molten, heated filled polymer encapsulant material into the die cavities to encapsulate the first and second semiconductor dice and preventing flow of the encapsulant from the die cavities past the primary lead fingers using the superimposed dam bars of the first and second offset lead frames and the primary lead frame.